REMARKS

In the February 17, 2004 Office Action, the Examiner rejected all of the claims pending in the application (claims 1-15). This Response amends claim 5. After entry of the above amendment, claims 1-15 (including four independent claims) remain pending in the application. Applicants request reconsideration of the application in view of the above amendment and the following remarks.

Claim 5 stands rejected under 35 U.S.C. §102(e) as being anticipated by Albonesi, U.S. Pat. No. 6,205,537 (hereinafter "Albonesi"). Applicants traverse this rejection.

Albonesi discloses a dynamically reconfigurable microprocessor having multiple processor elements. The processor elements disclosed by Albonesi are arranged in a linear configuration, and each element is controlled using a single control signal (see FIG. 4). In contrast, claim 5 is directed to power saving in an M row by N column processor. In particular, Claim 5 recites the step of "masking an MxN array of processor cells to enable a subset of cells." Albonesi does not disclose an MxN processor array or the masking of such an array to enable active cells and to disable inactive cells such that they do not consume power.

For at least the above reasons, Albonesi does not anticipate the invention of claim 5 and Applicants request the withdrawal of the §102(e) rejection of claim 5.

Claims 1-4 and 6-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Albonesi in view of Morton, U.S. Pat. No. 4,907,148 (hereinafter "Morton"). Applicants traverse this rejection.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the reference or to combine the references as proposed by the Examiner. Second, there must be a reasonable expectation of success. Third, the prior art reference or references must teach or suggest all the claim limitations. Applicants submit that the Examiner has not satisfied all of the basic criteria set forth above.

Regarding claim 1, the combination of Albonesi and Morton does not teach or suggest each and every claim limitation. More specifically, the combination does not teach or suggest the step of "gating the row mask signal and column mask signal with a clock signal of each cell" as recited in claim 1. Morton actually teaches away from this limitation as evidenced by the array processor cell shown in Morton's FIG. 4, which continues to receive and operate on at least one clock signal regardless of its "active" or "inactive" status. Applicants respectfully disagree with the Examiner's allegation that it would have been obvious to modify Albonesi to support the rejection of claim 1. As mentioned above, Albonesi does not disclose an MxN

processor array. Nor does Albonesi disclose the use of row and column mask signals. Consequently, Applicants submit that it would not have been obvious to use the clock signal of Albonesi to gate row and column mask signals that were not even contemplated by Albonesi.

Furthermore, one skilled in the art would not be motivated to combine Albonesi and Morton. For example, the processor of Morton is intended to overcome prior art processors where "only a single control bit per cell" is provided (Column 2, Lines 20-22). Albonesi, however, discloses such a processor architecture, i.e., one where each element is enabled/disabled with one control signal (see FIG. 4 of Albonesi). Accordingly, Morton teaches away from the control signal methodology of Albonesi and one skilled in the art would not be motivated to make the proposed combination.

For at least the above reasons, claim 1, and claims 2-4, which variously depend from claim 1, are not unpatentable over Albonesi in view of Morton. Therefore, Applicants request the withdrawal of the §103(a) rejection of those claims.

Regarding claim 6, the combination of Albonesi and Morton does not teach or suggest each and every claim limitation. For the reasons discussed above in connection with claim 1, the combination does not teach or suggest "a clock circuit, connected to supply each cell with a clock signal, each clock signal being gated with the row mask signal and column mask signal" as recited in claim 6. In addition, for the reasons discussed above in connection with claim 1, one skilled in the art would not be motivated to combine Albonesi and Morton.

For at least the above reasons, claim 6, and claims 7-10, which variously depend from claim 6, are not unpatentable over Albonesi in view of Morton. Therefore, Applicants request the withdrawal of the §103(a) rejection of those claims.

Regarding claim 11, the combination of Albonesi and Morton does not teach or suggest each and every claim limitation. For the reasons discussed above in connection with claim 1, the combination does not teach or suggest "a clock for providing a clock signal, the clock signal being gated with the mask signal" as recited in claim 11. In addition, for the reasons discussed above in connection with claim 1, one skilled in the art would not be motivated to combine Albonesi and Morton.

For at least the above reasons, claim 11, and claims 12-15, which variously depend from claim 11, are not unpatentable over Albonesi in view of Morton. Therefore, Applicants request the withdrawal of the §103(a) rejection of those claims.

No fee is due in connection with the filing of this Response. Nonetheless, in an abundance of caution, the Commissioner is hereby authorized to charge any fees that may be associated with this communication to Deposit Account No. 50/2258.

Respectfully submitted,

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